IN THE CLAIMS:

Please amend claims 1, 3, 5, 11, 15, and 19 as shown in the complete list of claims that is presented below.

1. (currently amended) An ESD protection apparatus for dual-polarity input pad, comprising:

a first region of a first conductivity type;

a second region of a second conductivity type opposite to said first conductivity type formed in said first region;

a third region of said first conductivity type formed in said second region;

a first input connection region of said first conductivity type and a second input connection region of said second conductivity type both formed in said third region; and

a first ground connection region of said first conductivity type and a second ground connection region of said second conductivity type both formed ~~on~~ in said first region, at locations that do not overlap the second region or the third region.

2. (original) An ESD protection apparatus of claim 1, further comprising a bridge region of said second conductivity type across said second region and extending to said first and third regions.

3. (currently amended) An ESD protection apparatus of claim 1, wherein said first region is ~~from~~ provided by a semiconductor substrate.

4. (original) An ESD protection apparatus of claim 1, wherein said first, second, and third regions are arranged in a triple-well manner.

5. (currently amended) An ESD protection apparatus of claim 1, wherein said first and second input connection regions are connected to ~~said~~ an input pad, and said first and second ground connection regions are connected to a ground pad.

6. (original) An ESD protection apparatus of claim 1, wherein said first input connection region, third region, second region, first region, and first and second ground connection regions form an SCR circuit under a positive polarity ESD event.

7. (original) An ESD protection apparatus of claim 1, wherein said first and second input connection regions, third region, second region, first region, and first ground connection region form an SCR circuit under a negative polarity ESD event.

8. (original) An ESD protection apparatus of claim 1, wherein said first, second and third regions form two back-to-back diodes under a normal operation.

9. (original) An ESD protection apparatus of claim 2, wherein said bridge region breaks down to said first region under a positive polarity ESD event.

10. (original) An ESD protection apparatus of claim 2, wherein said bridge region breaks down to said third region under a negative polarity ESD event.

11. (currently amended) An ESD protection apparatus for dual-polarity input pad, comprising:

an SCR structure including a first and a second semiconductor regions of a first conductivity type, and ~~inserted with~~ a third semiconductor region of a second conductivity type opposite to said first conductivity type inserted therebetween;

a first electrode region connected to said first semiconductor region, said first electrode region having a first part of said first conductivity type and a second part of said second conductivity type; and

a second electrode region connected to said second semiconductor region, said second electrode region having a first part of said first conductivity type and a second part of said second conductivity type.

12. (original) An ESD protection apparatus of claim 11, further comprising a PN junction breaking down to said first semiconductor region under a positive polarity ESD event.

13. (original) An ESD protection apparatus of claim 11, further comprising a PN junction breaking down to said second semiconductor region under a negative polarity ESD event.

14. (original) An ESD protection apparatus of claim 11, wherein said SCR structure is formed by CMOS triple-well process.

15. (currently amended) An ESD protection apparatus of claim 11, wherein said first and second parts of said first electrode region are connected to a ground pad, and said first and second parts of said second electrode region are connected to ~~said~~ an input pad.

16. (original) An ESD protection apparatus of claim 11, wherein said first part of said second electrode region, second semiconductor region, third semiconductor region, first semiconductor region, and first and second parts of said first electrode region form an SCR circuit under a positive polarity ESD event.

17. (original) An ESD protection apparatus of claim 11, wherein said first and second parts of said second electrode region, second semiconductor region, third semiconductor region, first semiconductor region, and first part of said first electrode region form an SCR circuit under a negative polarity ESD event.

18. (original) An ESD protection apparatus of claim 11, wherein said first semiconductor region, third semiconductor region, and second semiconductor region form two back-to-back diodes under a normal operation.

19. (currently amended) An ESD protection method for dual-polarity input pad, comprising the steps of:

forming a first and second semiconductor regions of a first conductivity type, ~~inserted with~~ and a third semiconductor region of a second conductivity type opposite to said first conductivity type inserted therebetween;

forming a first electrode region having a first part of said first conductivity type and a second part of said second conductivity type both connected to said first semiconductor region;

forming a second electrode region having a first part of said first conductivity type and a second part of said second conductivity type both connected to said second semiconductor region;

connecting said first electrode region to said input pad; and

connecting said second electrode region to a ground pad.

20. (original) An ESD protection method of claim 19, wherein said first, second and third semiconductor regions are formed by CMOS triple-well process.

21. (original) An ESD protection method of claim 19, further comprising forming a bridge region of said second conductivity type across said third semiconductor region and extending to said first and second semiconductor regions.

22. (original) An ESD protection method of claim 19, further comprising forcing a junction breakdown at said second semiconductor region under a positive polarity ESD event.

23. (original) An ESD protection method of claim 19, further comprising forcing a junction breakdown at said first semiconductor region under a negative polarity ESD event.

24. (original) An ESD protection method for dual-polarity input pad, comprising the steps of:

forming an SCR structure;

connecting a first electrode region having regions of opposite conductivity types to said SCR structure;

connecting a second electrode region having regions of opposite conductivity types to said SCR structure;

connecting said first electrode region to said input pad; and

connecting said second electrode region to a ground pad.

25. (original) An ESD protection method of claim 24, wherein said SCR structure is formed by CMOS triple-well process.

26. (original) An ESD protection method of claim 24, further comprising forcing a junction breakdown to lower a triggering voltage of said SCR structure under a positive polarity ESD event.

27. (original) An ESD protection method of claim 24, further comprising forcing a junction breakdown to lower a triggering voltage of said SCR structure under a negative polarity ESD event.